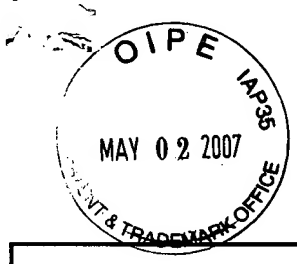
AF 2871/TON



PTO/SB/21 (08-00)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission	

Application Number	09/285,899
Filing Date	April 8, 1999
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2871
Examiner Name	M. Ton
Attorney Docket Number	0756-1950

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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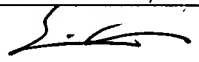
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosures
  1. Response to Notification of Non-Compliant Appeal Brief
  2.
  3.

Remarks

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Eric J. Robinson, Reg. No. 38,285 Robinson Intellectual Property Law Office, P.C. PMB 955 21010 Southbank Street Potomac Falls, VA 20165
Signature	
Date	April 30, 2007

CERTIFICATE OF MAILING

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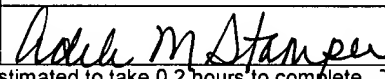
Type or printed name	Adele M. Stamper		
Signature		Date	April 30, 2007

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Attorney Docket No. 0756-1950

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2871
Shunpei YAMAZAKI et al.	)	Examiner: Minh Toan T. Ton
Serial No. 09/285,899	)	CERTIFICATE OF MAILING
Filed: April 9, 1999	)	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 30, 2007.
For: ELECTRO-OPTICAL DEVICE HAVING LEVELING FILM	)	Ashlee M Stamper

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The *Notification of Non-Compliant Appeal Brief* mailed March 29, 2007, has been received and its contents carefully noted. This response is filed within two months of the mailing date of the *Notification* and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

Initially, the Applicant appreciates Ms. Brown's time in conducting a telephonic interview on April 5, 2007. Regarding the *Appeal Brief* filed July 10, 2006 (received by OIPE July 13, 2006), the *Notification* asserts that the Status of Claims (Section III) does not include a statement identifying the claims on appeal, and that the Summary of Claimed Subject Matter (Section V) does not "map the independent claims on appeal to the specification by page, and line number and to the drawings" (Paper No. 20070328). In response, as agreed, the Appellant has attached a revised Status of Claims (Section III) and a revised Summary of Claimed Subject Matter (Section V).

III. STATUS OF THE CLAIMS

Claims 9-16, 21-24, 33-36, 50-52, 54 and 57-97 are pending in the present application, of which claims 9, 13, 21, 33, 57-59, 66, 69, 73, 77, 81, 85, 89 and 93 are independent. Claims 69-97 have been withdrawn from consideration (page 2, Paper No. 08042005). Accordingly, claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68 are currently elected, of which claims 9, 13, 21, 33, 57-59 and 66 are independent. No claims have been deemed allowable by the examiner. The Appellants appeal the rejection of claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 9, 13 and 57 relate to a device having at least one liquid crystal panel (e.g. Figures 7(A)-(I) and 12(A)-(E)), the liquid crystal panel comprising a first substrate (e.g. 50) having an insulating surface; a second substrate (e.g. 80) being opposed to the first substrate; at least one thin film transistor or semiconductor element (e.g. 63 or 64) being formed over the first substrate, the thin film transistor or semiconductor element including at least a channel region, source and drain regions (e.g. 55, 56 or 59, 60) with the channel region therebetween, a gate insulating film (e.g. 65) adjacent to the channel region and a gate electrode (e.g. 66 or 67) adjacent to the channel region with the gate insulating film interposed therebetween; where the channel region, the source and drain region of the one thin film transistor or semiconductor element is formed in a semiconductor island; an organic resin or leveling film (e.g. 77) formed over the first substrate to provide a leveled upper surface over the first substrate, the organic resin or leveling film covering the thin film transistor or semiconductor element; a pixel electrode (e.g. 71) formed on the leveled upper surface, the pixel electrode being electrically connected to the thin film transistor or semiconductor element through an opening (e.g. Figure 7(H); page 14, lines 28-29; formed by mask P7) formed in the organic resin or leveling film; a liquid crystal material having ferroelectricity or antiferroelectricity (e.g. page 36, lines 2-6) and being formed between the first substrate and the second substrate; and an opposed electrode (e.g. 90) formed over the second substrate and opposed to the pixel electrode with the liquid crystal material interposed therebetween.

Independent claims 21 and 58 relate to a television (e.g. Figure 9) comprising a tuner (e.g. 223) for receiving television radio waves; liquid crystal panel (e.g. Figures 7(A)-(I) and 12(A)-(E)) operationally connected to the tuner; the liquid crystal panel comprising a first substrate (e.g. 50) having an insulating surface; a second substrate (e.g. 80) being opposed to the first substrate; at least one thin film transistor (e.g. 63 or 64) being formed over the first substrate, the thin film transistor including at least a channel region, source and drain regions (e.g. 55, 56 or 59, 60) with the channel region therebetween, a gate insulating film (e.g. 65) adjacent to the channel region and a gate electrode (e.g. 66 or 67) adjacent to the channel region with the gate insulating film interposed therebetween; where the channel region, the source and drain region of the one thin film transistor is formed in a semiconductor island; an organic resin or leveling film (e.g. 77) formed over the first substrate to provide a leveled upper surface over the first substrate, the organic resin or leveling film covering the thin film transistor; a pixel electrode (e.g. 71) formed on the leveled upper surface, the pixel electrode being electrically connected to the thin film transistor through an opening (e.g. Figure 7(H); page 14, lines 28-29; formed by mask P7) formed in the organic resin or leveling film; a liquid crystal material having ferroelectricity or antiferroelectricity (e.g. page 36, lines 2-6) and being formed between the first substrate and the second substrate; and an opposed electrode (e.g. 90) formed over the second substrate and opposed to the pixel electrode with the liquid crystal material interposed therebetween.

Independent claims 33 and 59 relate to a portable computer (e.g. Figure 20) having a liquid crystal panel (e.g. Figures 7(A)-(I) and 12(A)-(E)), the liquid crystal panel comprising a first substrate (e.g. 50) having an insulating surface; a second substrate (e.g. 80) being opposed to the first substrate; at least one thin film transistor (e.g. 63 or 64) being formed over the first substrate, the thin film transistor including at least a channel region, source and drain regions (e.g. 55, 56 or 59, 60) with the channel region therebetween, a gate insulating film (e.g. 65) adjacent to the channel region and a gate electrode (e.g. 66 or 67) adjacent to the channel region with the gate insulating film interposed therebetween; where the channel region, the source and drain region of the one thin film transistor is formed in a semiconductor island; an organic resin or leveling film (e.g. 77) formed over the first substrate to provide a leveled upper surface over the

first substrate, the organic resin or leveling film covering the thin film transistor; a pixel electrode (e.g. 71) formed on the leveled upper surface, the pixel electrode being electrically connected to the thin film transistor through an opening (e.g. Figure 7(H); page 14, lines 28-29; formed by mask P7) formed in the organic resin or leveling film; a liquid crystal material having ferroelectricity or antiferroelectricity (e.g. page 36, lines 2-6) and being formed between the first substrate and the second substrate; and an opposed electrode (e.g. 90) formed over the second substrate and opposed to the pixel electrode with the liquid crystal material interposed therebetween.

Independent claim 66 relates to a projector (e.g. Figure 17) having at least one liquid crystal panel (e.g. Figures 7(A)-(I) and 12(A)-(E)), the liquid crystal panel comprising a first substrate (e.g. 50) having an insulating surface; a second substrate (e.g. 80) being opposed to the first substrate; at least one thin film transistor (e.g. 63 or 64) being formed over the first substrate, the thin film transistor including at least a channel region, source and drain regions (e.g. 55, 56 or 59, 60) with the channel region therebetween, a gate insulating film (e.g. 65) adjacent to the channel region and a gate electrode (e.g. 66 or 67) adjacent to the channel region with the gate insulating film interposed therebetween; where the channel region, the source and drain region of the one thin film transistor is formed in a semiconductor island; a leveling film (e.g. 77) formed over the first substrate to provide a leveled upper surface over the first substrate, the leveling film covering the thin film transistor; a pixel electrode (e.g. 71) formed on the leveled upper surface, the pixel electrode being electrically connected to the thin film transistor through an opening (e.g. Figure 7(H); page 14, lines 28-29; formed by mask P7) formed in the leveling film; a liquid crystal material having ferroelectricity or antiferroelectricity (e.g. page 36, lines 2-6) and being formed between the first substrate and the second substrate; and an opposed electrode (e.g. 90) formed over the second substrate and opposed to the pixel electrode with the liquid crystal material interposed therebetween.

Should anything further be desirable to place this application in better condition for review by the Board, please contact the undersigned at the telephone number listed below.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

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